Claims

1. A method for simulating hardware parallelism, the method comprising the steps of:

providing a plurality of hardware objects, each representing at least a portion of a design of a hardware device;

providing an interconnection object in communication with (i) at least a first hardware object and (ii) at least a second hardware object, the interconnection object including a source variable and a destination variable;

storing, by the at least one interconnection object, output data from the at least one first hardware object in the source variable, the output data being intended for receipt by the at least one second hardware object;

setting the destination variable equal to the source variable based at least in part on receipt of an update command; and

causing the at least one second hardware object to receive data from the destination variable as input.

2. The method of claim 1 wherein the at least one first hardware object and the at least one second hardware object are the same hardware object.

3. The method of claim 1 wherein the output data is based at least in part on a plurality of values supplied by the at least one first hardware object.

4. The method of claim 1 wherein the output data is based at least in part on a random function.

5. The method of claim 1 wherein the output data is based at least in part on a resolution function.

6. The method of claim 1 wherein the source variable comprises output data from a plurality of hardware objects.

7. The method of claim 1 wherein the update command is received after a signal transition.

8. The method of claim 7 wherein the signal transition comprises a clock pulse.

9. The method of claim 7 wherein the signal transition comprises a reset.

10. The method of claim 7 wherein the signal transition is based at least in part on an arbitrary function.

11. The method of claim 1 wherein the at least one first hardware object and the at least one second hardware object reside within separate computational processes.

12. The method of claim 1 wherein the at least one first hardware object and the at least one second hardware object are executed by different processors.

13. The method of claim 1 wherein the at least one first hardware object and the at least one second hardware object reside on different computers.

14. The method of claim 1 wherein the source variable contains a plurality of source data values.

15. The method of claim 14 further comprising the step of detecting illegal source data values and preventing their storage in the source variable.

16. The method of claim 14 wherein the plurality of source data values comprises a plurality of states of at least one pin of a hardware device corresponding to the at least one first hardware object.

17. The method of claim 14 wherein the plurality of source data values comprises at least one state of a plurality of pins of at least one hardware device corresponding to the at least one first hardware object.

18. The method of claim 14 wherein the at least one first hardware object corresponds to at least one bus, the plurality of source data values comprising a plurality of states of the at least one bus.

19. The method of claim 14 wherein the plurality of source data values comprises at least one state of a plurality of buses.

20. The method of claim 19 further comprising the step of providing a resolution function to accommodate multiple drivers for a single bus or signal.

21. The method of claim 14 wherein the plurality of source data values comprises a plurality of states of at least one control signal coming from the at least one first hardware object.

22. The method of claim 14 wherein the plurality of source data values comprises at least one state of a plurality of control signals coming from the at least one first hardware object.

23. The method of claim 1 wherein the destination variable contains a plurality of destination data values.

24. The method of claim 23 further comprising the step of detecting illegal destination data values and preventing their storage in the destination variable.

25. The method of claim 23 wherein the plurality of destination data values comprises a plurality of states of at least one pin of the at least one second hardware object.

26. The method of claim 23 wherein the plurality of destination data values

comprises at least one state of a plurality of pins of the at least one second hardware object.

27. The method of claim 23 wherein the plurality of destination data values comprises a plurality of states of at least one bus.

28. The method of claim 23 wherein the plurality of destination data values comprises at least one state of each of a plurality of buses.

29. The method of claim 28 further comprising the step of providing a resolution function to accommodate different bus types.

30. The method of claim 23 wherein the plurality of destination data values comprises a plurality of states of at least one control signal going to the at least one second hardware object.

31. The method of claim 23 wherein the plurality of destination data values comprises at least one state of a plurality of control signals going to the at least one second hardware object.

32. An apparatus for simulating hardware parallelism, the apparatus comprising:

at least one first hardware object and at least one second hardware object, each hardware object representing at least a portion of a design of a hardware device;

at least one interconnection object in communication with the at least one first hardware object and the at least one second hardware object, wherein the at least one interconnection object includes a source variable and a destination variable and is responsive to an update command, the interconnection object being configured to (i) receive, in the source variable, output data from the at least one first hardware object intended for receipt by the at least one second hardware object, (ii) set the destination variable equal to the source variable based at

least in part on receipt of the update command, and (iii) thereupon provide to the at least one second hardware object data from the destination variable as input.

33. The apparatus of claim 32 wherein the first hardware object and the second hardware object are the same hardware object.

34. The apparatus of claim 32 wherein the output data is based at least in part on a plurality of values supplied by the first hardware object.

35. The apparatus of claim 32 wherein the interconnection object comprises means for processing the output data based at least in part on a randomized function.

36. The apparatus of claim 32 wherein the interconnection object comprises means for processing the output data based at least in part on a resolution function.

37. The apparatus of claim 32 wherein the at least one first hardware object and the at least one second hardware object reside within separate computational processes.

38. The apparatus of claim 32 wherein the at least one first hardware object and the at least one second hardware object are executed by different processors.

39. The apparatus of claim 32 wherein the at least one first hardware object and the at least one second hardware object reside on different computers.

40. The apparatus of claim 32 wherein the source variable is configured to accommodate a plurality of source data values.

41. The apparatus of claim 32 wherein the interconnection object comprises means for detecting illegal source data values and preventing their storage in the source variable.

42. The apparatus of claim 40 wherein the at least one first hardware object corresponds to a device comprising at least one pin, the plurality of source data values comprising a plurality of states of the at least one pin of the hardware device corresponding to the at least one first hardware object.

43. The apparatus of claim 40 wherein the at least one first hardware object corresponds to a bus, the output data comprising a plurality of states of the bus.

44. The apparatus of claim 43 wherein the interconnection object comprises means for executing a resolution function to accommodate different bus types.

45. The apparatus of claim 40 wherein the output data comprises a plurality of states of a control signal coming from the at least one first hardware object.

46. The apparatus of claim 45 wherein the plurality of source data values comprises a plurality of control signals coming from the at least one first hardware object.

47. The apparatus of claim 32 wherein the destination variable is configured to accommodate a plurality of destination data values.

48. The apparatus of claim 47 wherein the at least one second hardware object corresponds to a device comprising at least one pin, the plurality of destination data values comprising a plurality of states of the at least one pin of the hardware device corresponding to the at least one second hardware object.

49. The apparatus of claim 47 wherein the plurality of destination data values comprises a plurality of states of a bus.

50. The apparatus of claim 47 wherein the plurality of destination data values

comprises a state of each of a plurality of buses.

51. The apparatus of claim 50 wherein the interconnection object comprises means for executing a resolution function to accommodate multiple drivers for a single bus or signal.

52. The apparatus of claim 47 wherein the plurality of destination data values comprises a plurality of states of a control signal going to the at least one second hardware object.

53. The apparatus of claim 47 wherein the plurality of destination data values comprises a state of a plurality of control signals going to the at least one second hardware object.